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PATENT NUMBER

## U.S. UTILITY Patent Application

JCSRY

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**O.I.P.E.**

**PATENT DATE**

**SCANNED**

**Q.A.**

Q.A. Am

APPLICATION NO. 09/683872	CONT/PRIOR	CLASS 257	SUBCLASS 459	ART UNIT 2811 2815	EXAMINER C. L. Lee
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Joseph Ladanza

Arth

**TITLE**

## Method of connecting core I/O pins to backside chip I/O pads

PTO-2040  
12/89

## ISSUING CLASSIFICATION

[illegible]

<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b> <div> <div>Sheets Drwg.</div> <div>Figs. Drwg.</div> <div>Print Fig.</div> </div>		<b>CLAIMS ALLOWED</b>	
			Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) (Date)		<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____			<b>ISSUE FEE</b>	
	Amount Due	Date Paid		
<input type="checkbox"/> The terminal ____ months of this patent have been disclaimed.	_____ (Legal Instruments Examiner) (Date)		<b>ISSUE BATCH NUMBER</b>	

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